**Abstract**

A channelization code is generated in response to a spreading factor and a code number. The code number is right justified to provide a right-justified code number. The right-justified code number is stored in an eight-bit register. An eight-bit binary counter is arranged to provide a binary count. The binary counter is reset when the binary count reaches a value equal to the spreading factor minus one. A channelization logic circuit is configured to convert the binary count and the stored right-justified code number into the channelization code. According to one example, the channelization logic circuit comprises eight AND gates and eight XOR gates. A channelization code generator circuit may be integrated into an integrated chip that has a small silicon area and low power consumption.

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